

	L #	Hits	Search Text	DBs
1	L1	14035	(scatter\$3 gather\$3) near10 (bit byte element item)	USPAT; US-PGPUB
2	L3	5584	(scatter\$3 gather\$3) near10 (bit byte element item)	EPO; JPO; DERWENT
3	L2	144	1 near20 mask\$3	USPAT; US-PGPUB
4	L4	44	3 near20 mask\$3	EPO; JPO; DERWENT; IBM TDB
5	L6	2739	(scatter\$3 gather\$3) near20 mask\$3	USPAT; US-PGPUB
6	L10	47646	(reorder\$3 order\$3 rearrang\$3 arang\$3) near10 (bit byte element item)	EPO; JPO; DERWENT; IBM TDB
7	L11	1026	(scatter\$3 gather\$3) near20 mask\$3	EPO; JPO; DERWENT; IBM TDB
8	L12	4	10 and 11	EPO; JPO; DERWENT; IBM TDB
9	L9	103	(reorder\$3 order\$3 rearrang\$3 arang\$3 scatter\$3 gather\$3).ab,ti. and 7	USPAT; US-PGPUB
10	L13	351267	(reorder\$3 order\$3 rearrang\$3 arrang\$3) near10 (bit byte element item)	USPAT; US-PGPUB
11	L14	170489	(reorder\$3 order\$3 rearrang\$3 arrang\$3) near10 (bit byte element item)	EPO; JPO; DERWENT; IBM TDB
12	L16	593	6 and 13	USPAT; US-PGPUB
13	L18	15	11 and 14	EPO; JPO; DERWENT; IBM TDB
14	L17	171	(reorder\$3 order\$3 rearrang\$3 arrang\$3 scatter\$3 gather\$3).ab,ti. and 16	USPAT; US-PGPUB

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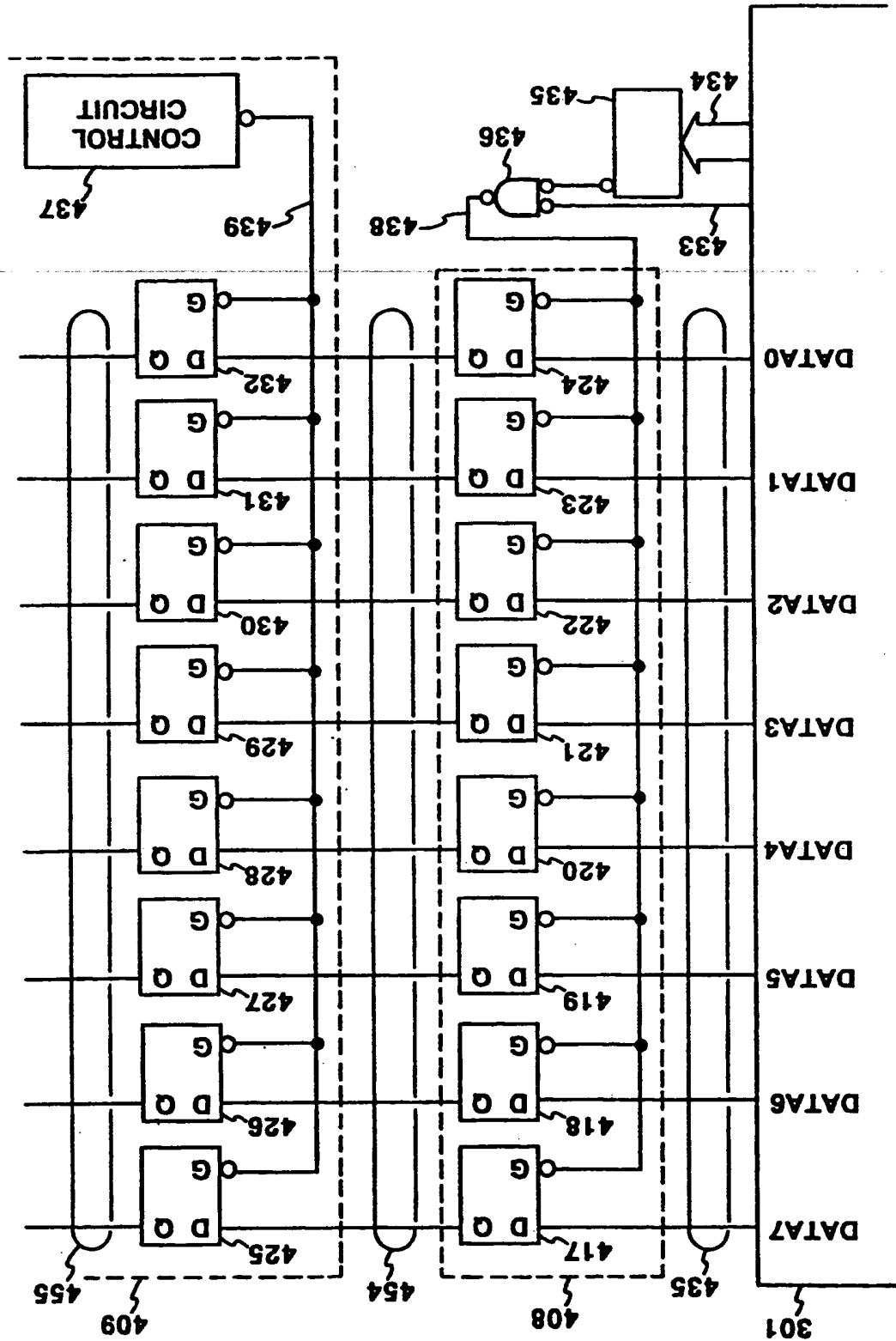
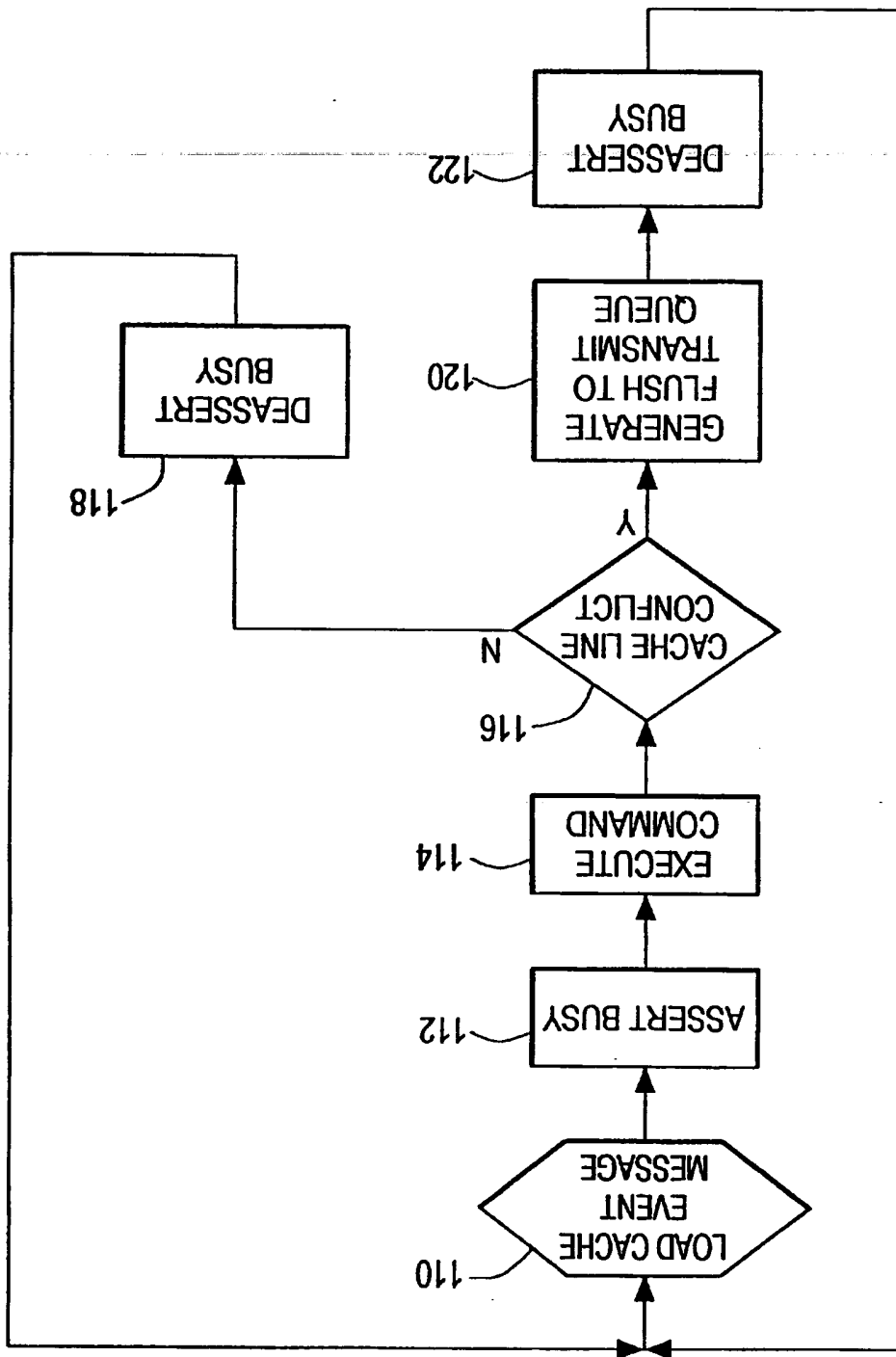


FIG. 35 (PRIOR ART)

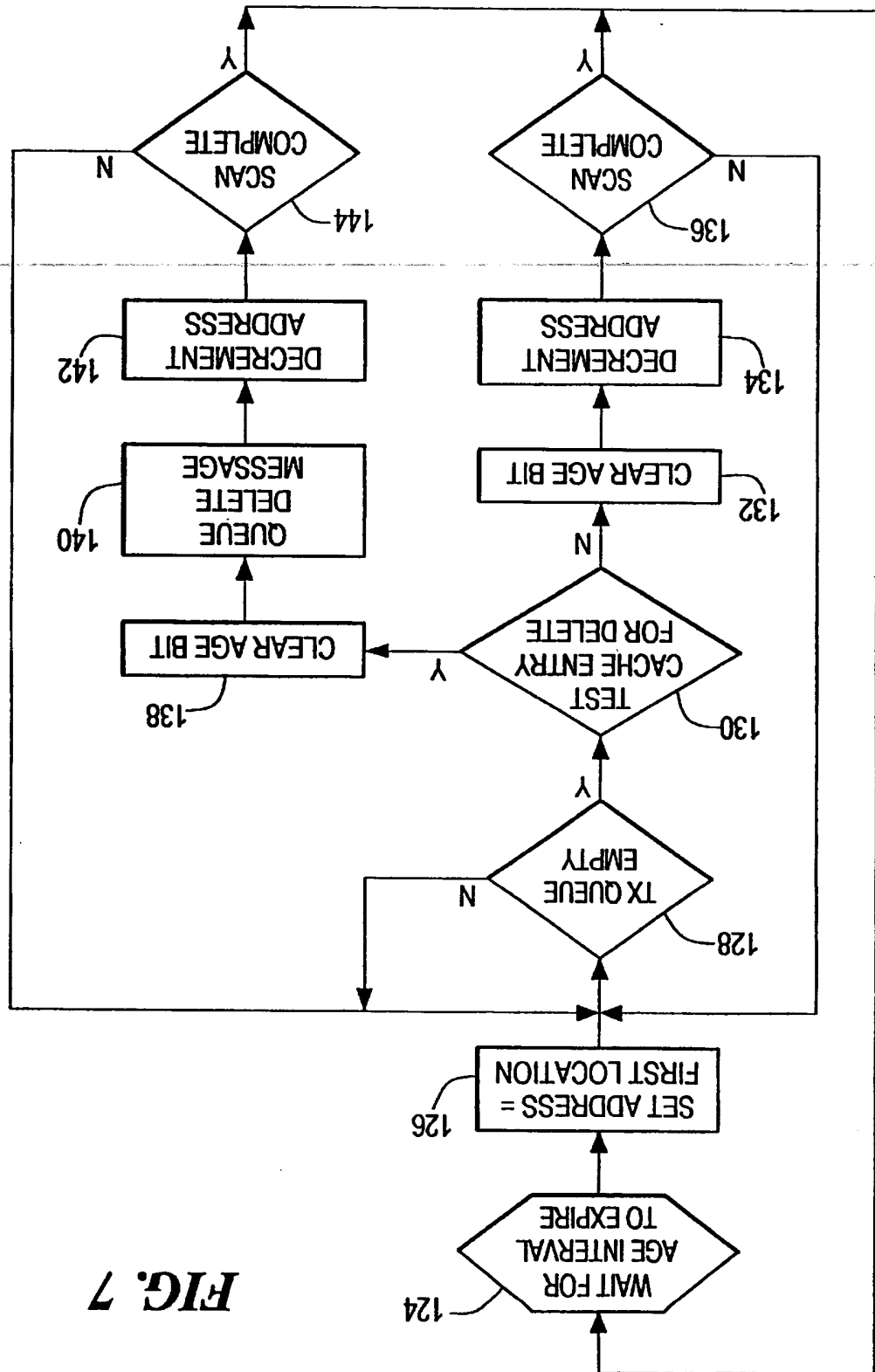
	Docum ent ID	U	Title	Current OR
1	JP 20020 96461 A	<input type="checkbox"/>	DEVICE FOR IMAGE RECORDING, METHOD FOR CONTROLLING IMAGE RECORDING, AND RECORDING MEDIUM	
2	JP 10096 700 A	<input type="checkbox"/>	APPARATUS FOR INSPECTING FOREIGN MATTER	
3	JP 08201 313 A	<input type="checkbox"/>	DEFECT INSPECTION METHOD FOR TRANSPARENT PLATE-LIKE BODY AND DEVICE THEREOF	
4	JP 07198 625 A	<input type="checkbox"/>	PRINT INSPECTING SENSOR	
5	JP 05079 913 A	<input type="checkbox"/>	STRAY LIGHT FREE FOURIER SPECTROPHOTOMETER	
6	JP 05031 670 A	<input type="checkbox"/>	BLAST PROCESSING METHOD FOR METALLIC PRODUCT	
7	JP 04194 908 A	<input type="checkbox"/>	LIQUID CRYSTAL DISPLAY DEVICE	
8	JP 60024 568 A	<input type="checkbox"/>	COLOR TONER CONCENTRATION DETECTOR	
9	WO 96055 03 A1	<input type="checkbox"/>	DEVICE FOR TESTING OPTICAL ELEMENTS	
10	US 58447 22 A	<input type="checkbox"/>	Polarization beam splitter for colour projection system - has wave blocking element arranged at bottom edge of mask and immersed in prismatic fluid, for minimizing scattering of incident electromagnetic wave	
11	JP 10096 700 A	<input checked="" type="checkbox"/>	Inspection apparatus for detecting adhesion of foreign particles in mask used in exposure system of semiconductor device, LCD element manufacture - has optical correction element arranged in between mask and optical receiving unit that receives reflected light, to correct aberrational defects	
12	JP 09257 685 A	<input checked="" type="checkbox"/>	Photodetector for measuring particle size distribution in specimen - includes mask on light receiving surface to focus scattered light into fixed area of light receiving element	
13	US 52989 69 A	<input checked="" type="checkbox"/>	Combined optical train for laser spectroscopy - has first focussing lens located one focal length from centre of sample cell, second focussing lens one focal length ahead of aperture element, and optical masking element between two lenses	
14	EP 55665 5 A	<input checked="" type="checkbox"/>	Grading and evaluating method for optical elements such as lenses - scanning rotated linear wedge shaped beam of white light on entire lens surface and detecting defect scattered light using CCD via mask	
15	US 45989 97 A	<input checked="" type="checkbox"/>	Detector for defects and dust on semiconductor wafer or video disc - detects scattered light free of diffracted beams from pattern by mask with apertures blocking specular reflections	

FIG. 6



	Docum ent ID	U	Title	Current OR
1	US 20040 07876 3 A1	<input type="checkbox"/>	Short edge smoothing for enhanced scatter bar placement	716/2
2	US 20040 07505 3 A1	<input checked="" type="checkbox"/>	Particle-optical arrangements and particle-optical systems	250/310
3	US 20040 07312 0 A1	<input checked="" type="checkbox"/>	Systems and methods for spectroscopy of biological tissue	600/478
4	US 20040 05805 8 A1	<input checked="" type="checkbox"/>	Raman-active taggants and thier recognition	427/7
5	US 20040 04701 4 A1	<input checked="" type="checkbox"/>	In-line holographic mask for micromachining	359/15
6	US 20040 01194 8 A1	<input checked="" type="checkbox"/>	High accuracy miniature grating encoder readhead using fiber optic receiver channels	250/231 .13
7	US 20040 00834 3 A1	<input checked="" type="checkbox"/>	Electromagnetic radiation attenuating and scattering member with improved thermal stability	356/243 .1
8	US 20030 19139 8 A1	<input checked="" type="checkbox"/>	Systems and methods for spectroscopy of biological tissue	600/478
9	US 20030 15553 2 A1	<input checked="" type="checkbox"/>	Electron-beam lithography	250/492 .3
10	US 20030 11242 1 A1	<input checked="" type="checkbox"/>	Apparatus and method of image enhancement through spatial filtering	355/71
11	US 20030 10376 0 A1	<input checked="" type="checkbox"/>	OPTICAL ELEMENT HAVING PROGRAMMED OPTICAL STRUCTURES	385/146
12	US 20030 07752 1 A1	<input checked="" type="checkbox"/>	Method for producing scatter lines in mask structures for fabricating integrated electrical circuits	430/5
13	US 20030 07658 3 A1	<input checked="" type="checkbox"/>	Ultra-broadband UV microscope imaging system with wide range zoom capability	359/357
14	US 20030 07241 5 A1	<input checked="" type="checkbox"/>	Method for producing a scattered radiation grid or collimator	378/154
15	US 20030 06473 4 A1	<input checked="" type="checkbox"/>	Modified transmission method for improving accuracy for E-911 calls	455/456 .1
16	US 20030 05304 8 A1	<input checked="" type="checkbox"/>	Electron microscope and spectroscopy system	356/301
17	US 20030 03080 2 A1	<input checked="" type="checkbox"/>	MEASUREMENT OF PARTICLE SIZE DISTRIBUTION	356/336

FIG. 7



	Docum ent ID	U	Title	Current OR
18	US 20030 03078 3 A1	<input checked="" type="checkbox"/>	Consumable tube for use with a flow cytometry-based hematology system	356/39
19	US 20030 03005 5 A1	<input checked="" type="checkbox"/>	Color-filter substrate assembly, method for manufacturing the color-filter substrate assembly, electro-optical device, method for manufacturing electro-optical device, and electronic apparatus	257/72
20	US 20030 01951 8 A1	<input checked="" type="checkbox"/>	Photovoltaic element and process for the production thereof	136/256
21	US 20030 01685 4 A1	<input checked="" type="checkbox"/>	Radiation image processing apparatus, image processing system, radiation image processing method, storage medium, and program	382/132
22	US 20030 01172 2 A1	<input checked="" type="checkbox"/>	Method of fabricating near-field light-generating element	349/43
23	US 20020 18252 3 A1	<input checked="" type="checkbox"/>	Method for carrying out a rule-based optical proximity correction with simultaneous scatter bar insertion	430/30
24	US 20020 17183 1 A1	<input checked="" type="checkbox"/>	Polarized light scattering spectroscopy of tissue	356/369
25	US 20020 16372 9 A1	<input checked="" type="checkbox"/>	FIELD-OF-VIEW CONTROLLING ARRANGEMENTS	359/613
26	US 20020 16372 8 A1	<input checked="" type="checkbox"/>	Optical sheets or overlays	359/613
27	US 20020 08527 1 A1	<input checked="" type="checkbox"/>	Broad spectrum ultraviolet catadioptric imaging system	359/359
28	US 20020 05727 6 A1	<input checked="" type="checkbox"/>	Data processing apparatus, processor and control method	345/555
29	US 20020 03920 9 A1	<input checked="" type="checkbox"/>	IN-LINE HOLOGRAPHIC MASK FOR MICROMACHINING	359/15
30	US 20020 02549 0 A1	<input checked="" type="checkbox"/>	Raman-active taggants and their recognition	430/270 .15
31	US 20020 02464 3 A1	<input checked="" type="checkbox"/>	Projection exposure apparatus having aberration measurement device	355/52
32	US 20020 02145 1 A1	<input checked="" type="checkbox"/>	Scanning interferometric near-field confocal microscopy with background amplitude reduction and compensation	356/511
33	US 20010 04687 0 A1	<input checked="" type="checkbox"/>	Modified transmission method for improving accuracy for E-911 calls	455/456 .2
34	US 20010 02147 7 A1	<input checked="" type="checkbox"/>	Method of manufacturing a device by means of a mask phase-shifiting mask for use in said method	430/5

COHERENCE MECHANISM FOR DISTRIBUTED ADDRESS CACHE IN A NETWORK SWITCH

BACKGROUND OF THE INVENTION

The present invention is generally related to network switches, and more particularly to maintenance of consistency of data in segments of a distributed address cache in a network switch.

Network switches commonly employ an address cache to facilitate the flow of data units in a network. The address cache includes entries that indicate address information for various devices connected with the network such as computers and printers. In particular, the address information indicates which port or ports in the switch should be employed for forwarding the data unit to a particular device or group of devices in the network. Each data unit includes a header portion with a source address field and a destination address field. Following receipt of the data unit the switch attempts to locate an entry in the address cache that pertains to the destination address specified in the data unit header. If a pertinent entry is located in the address cache then the information contained in that entry is employed to cause transmission of the data unit via the specified port or ports associated with the address in order to "forward" the data unit toward the destination device. If a pertinent entry cannot be located in the address cache then the switch may "flood" the data unit by transmitting the data unit from every port except the port on which the data unit was received. Hence, network and switch bandwidth is conserved if a pertinent entry is available in the address cache.

It is known to update the address cache by "learning" new address information. Address information can be learned by employing the source address specified in the data unit header. If a first data unit is transmitted from a first device to a second device via the switch and the switch does not have the address for the first device in its address cache, then upon the initial transmission from the first device to the second device the switch learns the source address field of the first data unit. If address information for the second device is also unknown, the switch floods the first data unit in order to accomplish transmission to the second device. If the second device responds by transmitting a second data unit back to the first device via the switch then the switch learns the address of the second device from the source address field of the second data unit. The switch employs the learned address information for the first device to "forward" the second data and transmission from the first device to the second device the switch employs the learned address information for the second device to efficiently "forward" the data unit toward the second device via a single port without flooding the data unit through the network.

In an effort to ensure that the address cache contains accurate address information for active data flows, utilized entries in the address cache may be deleted in accordance with an "aging" technique. In particular, any entries that are not referenced in response to a source address search within a predetermined aging interval are deleted.

Input and output ("I/O") functions in a network switch are often implemented on Application Specific Integrated Circuits ("ASICs"). Because of limitations in the maximum practical size, a plurality of I/O ASICs may be employed in a single network switch device. Each I/O ASIC must have access to the address cache in order to enable learning.

BRIEF SUMMARY OF THE INVENTION

In accordance with the present invention, in a network switch device in which a distributed address cache having a plurality of cache segments is employed, events initiated at address cache segments of the distributed address cache, such as address learning operations, are serialized and contemporaneously shared and acted upon by the cache segments in order to maintain consistency throughout the distributed address cache.

The invention is predicated in part upon recognition that address cache learning operations are self repairing. For example, if address information for forwarding data units is not learned when a data unit is initially transmitted through the switch, the data unit and subsequent data units should nevertheless reach the destination device because flooding will be employed. Further, the address information can be learned from any subsequent data units transmitted by the same source device. Hence, "strict coherence," where each and every learning operation is implemented, is not required for switch operation, and consistency may be obtained with "weak coherence" by which some learning operations may be dropped (not implemented). The invention is also predicated in part upon recognition that address cache aging operations are self correcting. If an address cache entry is not removed after the first aging interval during which it was not referenced, it will be removed in a subsequent interval if it remains unused. Hence, "weak coherence" is also acceptable for aging operations.

Address cache update events (learning operations or aging operations) originate with a single segment of the distributed cache. The segment that initiates an update creates a cache event message and distributes it via an event sharing bus that interconnects all of the I/O ASICs. The event bus carries only one event message at a time; thus serializing event messages. An arbiter is employed to process requests for control of the event bus and to grant control to only one I/O ASIC at a time. When an address cache update event is

One known solution to the above described problem involves the use of a distributed address cache. The distributed address cache comprises a plurality of separate cache segments, each of which is associated with one particular I/O ASIC. The use of a distributed address cache simplifies the task of increasing the number of ports in the switch because the bandwidth required for address searching is limited by the number of ports supported by each ASIC rather than the number of ports in the entire switch.

However, implementing each and every learning, forwarding and aging operation is more complex when a distributed address cache is employed because different events occur simultaneously at different cache segments. Consequently, a situation will result where the segments will not each contain identical sets of entries. Such a loss of intersegment consistency has a deleterious effect on switch operation. Cache coherence algorithms can be applied to eliminate inconsistency among caches and preserve correct switch operation. Strict coherence mechanisms would require elaborate queuing methods and would impact the forwarding performance of the switch.

	Docum ent ID	U	Title	Current OR
35	US 20010 01640 4 A1	<input checked="" type="checkbox"/>	GaN substrate including wide low - defect region for use in semiconductor element	438/496
36	US 20010 01493 6 A1	<input checked="" type="checkbox"/>	Data processing device, system, and method using a table	711/221
37	US 67010 28 B1	<input checked="" type="checkbox"/>	Method and apparatus for fast signal convolution using spline kernel	382/279
38	US 66899 51 B2	<input checked="" type="checkbox"/>	Photovoltaic element and process for the production thereof	136/256
39	US 66895 45 B2	<input checked="" type="checkbox"/>	Method of fabricating near-field light-generating element	430/321
40	US 66861 38 B1	<input checked="" type="checkbox"/>	Color motion picture print film with improved raw stock keeping	430/505
41	US 66715 26 B1	<input checked="" type="checkbox"/>	Probe and apparatus for determining concentration of light-absorbing materials in living tissue	600/310
42	US 66678 09 B2	<input checked="" type="checkbox"/>	Scanning interferometric near-field confocal microscopy with background amplitude reduction and compensation	356/511
43	US 66467 42 B1	<input checked="" type="checkbox"/>	Optical device and method for multi-angle laser light scatter	356/342
44	US 66248 90 B2	<input checked="" type="checkbox"/>	Polarized light scattering spectroscopy of tissue	356/369
45	US 66181 74 B2	<input checked="" type="checkbox"/>	In-line holographic mask for micromachining	359/15
46	US 66103 51 B2	<input checked="" type="checkbox"/>	Raman-active taggants and their recognition	427/7
47	US 66097 99 B1	<input checked="" type="checkbox"/>	Field-of-view controlling arrangements	359/613
48	US 65446 94 B2	<input checked="" type="checkbox"/>	Method of manufacturing a device by means of a mask phase-shifting mask for use in said method	430/5
49	US 65206 49 B1	<input checked="" type="checkbox"/>	Image projection device and associated method	353/94
50	US 65194 65 B2	<input checked="" type="checkbox"/>	Modified transmission method for improving accuracy for E-911 calls	455/456 .1
51	US 65074 00 B1	<input checked="" type="checkbox"/>	Optical system for multi-part differential particle discrimination and an apparatus using the same	356/338
52	US 64983 51 B1	<input checked="" type="checkbox"/>	Illumination system for shaping extreme ultraviolet radiation used in a lithographic projection apparatus	250/492 .2
53	US 64905 30 B1	<input checked="" type="checkbox"/>	Aerosol hazard characterization and early warning network	702/24
54	US 64836 38 B1	<input checked="" type="checkbox"/>	Ultra-broadband UV microscope imaging system with wide range zoom capability	359/351
55	US 64769 10 B1	<input checked="" type="checkbox"/>	Light scattering apparatus and method for determining radiation exposure to plastic detectors	356/336
56	US 64632 90 B1	<input checked="" type="checkbox"/>	Mobile-assisted network based techniques for improving accuracy of wireless location system	455/456 .1

generated, the event is placed in an event message that is entered in a transmit queue in preparation for distribution via the event sharing bus. After queuing the event message, the I/O ASIC managing the cache segment asserts its request signal to the arbiter. When the arbiter grants control of the event bus, the event message is broadcast to all the ASICs via the event bus. Event messages that are received from the event bus are stored in a receive queue for processing. Once an event message has been received, each of the ASICs, including the originating ASIC, asserts a busy signal to the arbiter and processes the event. The busy signals prevent the arbiter from granting the event bus for another cache event message until all ASICs have completed processing the current event.

If a condition occurs at a distributed cache segment that warrants a cache update, but the transmit queue is full, a cache event message is not generated and the update is not performed. When an I/O ASIC completes processing of an event message from the receive queue, the cache line index of the message in the receive queue is compared against the cache line index of any message in the transmit queue. If a match is indicated, the cache event message in the transmit queue is flushed (deleted). Since the message is deleted before transmission of a cache event message, no cache segments are updated.

In accordance with one embodiment of the present invention the aging of entries in the distributed address cache may be dependent upon an ownership indicator. Each entry in the address cache includes an ownership field that indicates whether the cache segment in which the entry is stored is deemed to be the owner of the entry. The indicator is set such that the ASIC that generates the learn event that causes the entry to be stored in the cache segments is the sole owner of the entry. Only the owner of an entry is permitted to initiate an event that causes removal of the entry for aging. Aging of an entry is therefore determined by the cache segment with ownership rights to the entry.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The invention will be more fully understood from the following Detailed Description of the Invention, in conjunction with the Drawing of which:

FIG. 1 is a block diagram of a network switching device in accordance with the present invention;

FIG. 2 is a diagram that illustrates a segment of the distributed address cache;

FIG. 3 is a block diagram that illustrates use of the arbiter and event bus for serialization of distributed address cache events;

FIG. 4 is a flow diagram that illustrates a method for queuing learn events without impacting forwarding performance of the switch;

FIG. 5 is a flow diagram that illustrates control of a transmit queue;

FIG. 6 is a flow diagram that illustrates control of a receive queue; and

FIG. 7 is a flow diagram that illustrates an age scan process.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates a switch 10 that facilitates movement of data units in a network. The switch 10 includes a plurality of Input/Output Application Specific Integrated Circuits ("I/O

Referring to FIGS. 1 and 2, the address cache 24 is employed to facilitate processing of data units. More particularly, the address cache 24 includes entries that indicate address information that may be employed to transmit data units to various devices coupled to the network such as computers and printers. The address information includes an address indicator field and port index indexed by a particular device or group of devices. Following receipt of a data unit by I/O ASIC 12, for example, the address cache 24 is searched for an entry with an address indicator field that pertains to the destination address specified in the data unit header. If a pertinent entry is located in the address cache segment 24 then the port index contained in that entry is employed to cause transmission of the data unit via the specified port or ports in order to "forward" the data unit toward the destination device or devices. If a pertinent entry is not located in the address cache segment 24 then the switch 10 may "flood" the data unit by transmitting the data unit through every port in the switch except the port at which the data unit was received.

Referring again to FIG. 1, consistency is maintained between cache segments by synchronizing operations that affect the address information in the cache segments. In particular, distributed address cache update events such as address learning operations are serialized and contemporaneously acted upon in order to maintain consistency throughout the distributed address cache. An address cache update event may be initiated by any I/O ASIC, but the initiating I/O ASIC does not act upon the address cache update event, i.e., update the address cache associated with that I/O ASIC, until an event message is serialized and provided to all of the other I/O ASICs in the switch. Referring now to FIG. 3, in the illustrated embodiment address cache event messages are serialized and shared via the event sharing bus 20. The event sharing bus 20 is connected with an interface 21 in each I/O ASIC and an Arbiter device 42. The event bus 20 includes a shared data bus 48 and a control bus per I/O ASIC. As an example, the control bus for I/O ASIC 14 includes request line 44, grant line 46 and busy line 50. The physical limitations of the data bus 48 in the illustrated embodiment limit transmission to one event message at any point in time. Hence, in the illustrated embodiment address cache event messages which are broadcast via the data bus 48 are serialized. The arbiter device 42 is employed to manage the event sharing bus 20. When an event message is generated as a result of activity at an I/O ASIC, the event message is placed

	Docum ent ID	U	Title	Current OR
57	US 64490 23 B2	<input checked="" type="checkbox"/>	Active matrix liquid crystal display device	349/62
58	US 64479 59 B1	<input checked="" type="checkbox"/>	Amplitude mask for writing long-period gratings	430/5
59	US 64435 79 B1	<input checked="" type="checkbox"/>	Field-of-view controlling arrangements	359/613
60	US 64406 54 B1	<input checked="" type="checkbox"/>	Photographic element containing an electrically-conductive layer	430/529
61	US 64406 15 B1	<input checked="" type="checkbox"/>	Method of repairing a mask with high electron scattering and low electron absorption properties	430/5
62	US 64373 53 B1	<input checked="" type="checkbox"/>	Particle-optical apparatus and process for the particle-optical production of microstructures	250/492 .23
63	US 64207 14 B1	<input checked="" type="checkbox"/>	Electron beam imaging apparatus	250/396 ML
64	US 64080 49 B1	<input checked="" type="checkbox"/>	Apparatus, methods, and computer programs for estimating and correcting scatter in digital radiographic and tomographic imaging	378/98. 12
65	US 63777 26 B1	<input checked="" type="checkbox"/>	Transverse mode transformer	385/28
66	US 63625 15 B1	<input checked="" type="checkbox"/>	GaN substrate including wide low-defect region for use in semiconductor element	257/639
67	US 63340 59 B1	<input checked="" type="checkbox"/>	Modified transmission method for improving accuracy for e-911 calls	455/404 .2
68	US 63231 02 B1	<input checked="" type="checkbox"/>	Method of manufacturing a semiconductor device	438/424
69	US 63134 67 B1	<input checked="" type="checkbox"/>	Broad spectrum ultraviolet inspection methods employing catadioptric imaging	250/372
70	US 63046 26 B1	<input checked="" type="checkbox"/>	Two-dimensional array type of X-ray detector and computerized tomography apparatus	378/19
71	US 62951 20 B1	<input checked="" type="checkbox"/>	Position detection technique applied to proximity exposure	355/53
72	US 62854 39 B1	<input checked="" type="checkbox"/>	Position detection technique applied to proximity exposure	355/53
73	US 62485 10 B1	<input checked="" type="checkbox"/>	Motion picture intermediate film with process surviving antistatic backing layer	430/396
74	US 62464 51 B1	<input checked="" type="checkbox"/>	Stereoscopic image displaying method and stereoscopic image apparatus	349/15
75	US 62330 56 B1	<input checked="" type="checkbox"/>	Interferometric at-wavelength flare characterization of EUV optical systems	356/520
76	US 62330 43 B1	<input checked="" type="checkbox"/>	Position detection technique applied to proximity exposure	355/53
77	US 61779 94 B1	<input checked="" type="checkbox"/>	Relating to the measurement of particle size distribution	356/343
78	US 61772 37 B1	<input checked="" type="checkbox"/>	High resolution anti-scatter x-ray grid and laser fabrication method	430/320
79	US 61335 76 A	<input checked="" type="checkbox"/>	Broad spectrum ultraviolet inspection methods employing catadioptric imaging	250/461 .1

in an event transmit queue. For example, an event message generated at I/O ASIC 12 is placed in event transmit queue 52, and an event message 53 generated at I/O ASIC 14 is placed in event transmit queue 54. In the illustrated embodiment the event transmit queues 52, 54 will not accommodate more than one event message. If the event transmit queue 54 is empty when an event message is generated the event message 53 is loaded into the event transmit queue 54 and is discarded, resulting in no cache update. If the event message 53 is loaded into the event transmit queue 54, the I/O ASIC 14 asserts its event transmit queue 54 via the request line 44 of the bus 20. As previously described, the I/O ASIC 14 and associated address cache do not act upon the event message 53 before the event is distributed. The arbiter 42 is operative in response to the request for control of the event sharing bus from I/O ASIC 14 and any other I/O ASICs in the switch to apportion control of the data bus 48. In particular, the arbiter 42 processes the requests and grants control of the data bus 48 to one I/O ASIC at a time in accordance with predetermined criteria. When the arbiter 42 grants control of the data bus 48 to I/O ASIC 14, the event message 53 loaded in the bus 48 to I/O ASIC 14 is broadcast on the data bus 48 to each I/O ASIC in the switch. The event message 53 is received in event receive queue 60 of I/O ASIC 12, event receive queue 62 of I/O ASIC 14 and any other event receive queues in the switch. Each I/O ASIC acts upon the event message once the event message has been loaded into the respective receive queue in that I/O ASIC.

While acting upon the event message, such as by updating the address cache, the I/O ASIC asserts its busy signal to delay broadcast of further event messages. In response to assertion of the busy signal by any I/O ASIC the arbiter 42 delays granting control of the data bus 48 to any I/O ASIC. Hence, the start time for processing each new event message at each I/O ASIC is synchronized, thereby compensating for differences in the amount of time taken to process event messages at different I/O ASICs. This permits the receive queue to only implement storage for a single cache update message.

Cache update events are generated with a CIJ and CEI which indicate the memory location to update. Since event messages are queued for transmission, the state of the cache line may change between queuing of the event message on the transmit side and execution of the operation on the receive side. Conflict detection and resolution is employed to preserve consistency in the cache segments. The contents of both the event receive queue 62 and the event transmit queue 54 are provided to the conflict detector 64. The conflict detector 64 compares the queued event messages to determine if a conflict exists. A conflict exists when both event messages relate to the same cache line. The conflict detector indicates conflicts to the receive queue via signal line 65. As the last step in processing a message from the receive queue, the conflict line is sampled. If a conflict is indicated, the message in the transmit queue is flushed because it is based on stale cache line state.

A method for carrying out forwarding and learning operations is depicted in FIG. 4. The address cache is employed to identify ports to be used in forwarding a data unit received by an I/O ASIC. Initially, the received data unit is loaded into memory as indicated by step 70. The loaded data unit is examined to determine the specified destination address and 65 a pertinent entry as indicated by step 72. If no pertinent entry is located then the data unit is flooded to some or all of the output ports (other than the receive port) as indicated in step 74. If a pertinent entry is located then the data unit is transmitted via the specified port(s) as indicated by step 76. Address information is learned by employing the source address specified in the header of the data unit. As indicated by step 78, the loaded data unit is examined to determine the source address and the address cache is scanned to determine whether there is a pertinent entry. If a pertinent address cache entry is located then flow returns to step 70. If no pertinent address cache entry is located and the event transmit queue of the I/O ASIC is full as determined in step 80, flow returns to step 70. If no pertinent address cache entry is located and the event transmit queue of the I/O ASIC is not full as determined in step 80, a learn event message is generated and placed in the event transmit queue as indicated by step 82. Flow then returns to step 70.

Referring to FIGS. 2 and 7, an aging protocol is provided to remove unutilized address cache entries and to help ensure that the address cache contains accurate address information. Each cache entry includes an aging bit and an ownership bit. The ownership bit is only set in the entry in the cache segment that is connected with the I/O ASIC that caused the address cache entry to be installed via a learn operation. For the purposes of the present description, I/O ASIC 12 has ownership of the entry. In accordance with this embodiment of the aging protocol, a distributed cache entry can only be deleted via a message from the I/O ASIC with ownership of the entry (or a software generated management operation). When a data unit is received by the I/O ASIC 12 and an entry is located in the address cache segment 24 that matches the source address, the aging bit is set for that entry. After a predetermined interval has passed, the entries for which the aging bit is not set become eligible for deletion and all aging bits are reset. If the event transmit queue 52 is empty, and an entry is eligible for deletion, and the I/O ASIC 12 has ownership of the entry, then the entry is selected and a delete entry event message 88 is loaded into the event transmit queue 52. The delete entry event message 88 is broadcast via the data bus 48 and acted upon by each I/O ASIC when control of the data bus is granted to the I/O ASIC 12. If the event transmit queue is not empty the age scan process stalls and the next address entry is not scanned. When the transmit event queue is emptied, the age scan process continues.

A method for aging address cache entries is illustrated in FIG. 7. The method is initiated when the age interval expires as indicated by step 124. The address is then set to the first location. Flow loops until the transmit queue is empty as indicated by step 128, whereupon the cache entry is tested for a possible delete condition as indicated by step 130. Deletion occurs when age=0 and ownership=1. If the test result is negative, the age bit is cleared as indicated by step 132 and the address is decremented as indicated by step 134. If the scan is complete, as determined at step 136, flow returns to step 124. If the scan is not complete then flow returns to step 128. If the result of the tests at step 130 is affirmative, the age bit is cleared as indicated by step 138. A delete message is then queued as indicated by step 140 and the address is decremented as indicated by step 142. If the scan is complete as determined at step 144, flow returns to step 124. If the scan is not complete as determined at step 144, flow returns to step 128.

A method for controlling the transmit event queue is illustrated in FIG. 5. The process begins when a cache event message is queued for transmission as indicated by step 90.

	Docum ent ID	U	Title	Current OR
80	US 61181 59 A	<input checked="" type="checkbox"/>	Electrically programmable memory cell configuration	257/390
81	US 61153 44 A	<input checked="" type="checkbox"/>	Device and method for optical data storage having multiple optical states	369/100
82	US 61009 78 A	<input checked="" type="checkbox"/>	Dual-domain point diffraction interferometer	356/498
83	US 61009 71 A	<input checked="" type="checkbox"/>	Surface inspection tool	356/237 .2
84	US 60493 73 A	<input checked="" type="checkbox"/>	Position detection technique applied to proximity exposure	355/53
85	US 60347 76 A	<input checked="" type="checkbox"/>	Microroughness-blind optical scattering instrument.	356/369
86	US 60159 76 A	<input checked="" type="checkbox"/>	Fabrication apparatus employing energy beam	250/492 .23
87	US 60059 16 A	<input checked="" type="checkbox"/>	Apparatus and method for imaging with wavefields using inverse scattering techniques	378/87
88	US 59993 10 A	<input checked="" type="checkbox"/>	Ultra-broadband UV microscope imaging system with wide range zoom capability	359/351
89	US 59662 16 A	<input checked="" type="checkbox"/>	On-axis mask and wafer alignment system	356/401
90	US 59561 74 A	<input checked="" type="checkbox"/>	Broad spectrum ultraviolet catadioptric imaging system	359/357
91	US 59521 65 A	<input checked="" type="checkbox"/>	Topcoat for motion picture film	430/510
92	US 59404 68 A	<input checked="" type="checkbox"/>	Coded aperture X-ray imaging system	378/57
93	US 59332 30 A	<input checked="" type="checkbox"/>	Surface inspection tool	356/237 .2
94	US 59239 09 A	<input checked="" type="checkbox"/>	Distance measuring device and a camera using the same	396/114
95	US 59103 99 A	<input checked="" type="checkbox"/>	Backing layer for motion picture film	430/517
96	US 58895 80 A	<input checked="" type="checkbox"/>	Scanning-slit exposure device	355/67
97	US 58741 77 A	<input checked="" type="checkbox"/>	Strut aligning fixture	428/596
98	US 58689 52 A	<input checked="" type="checkbox"/>	Fabrication method with energy beam	216/66
99	US 58300 64 A	<input checked="" type="checkbox"/>	Apparatus and method for distinguishing events which collectively exceed chance expectations and thereby controlling an output	463/22
100	US 58074 48 A	<input checked="" type="checkbox"/>	Solid object generation	156/58
101	US 57988 27 A	<input checked="" type="checkbox"/>	Apparatus and method for determination of individual red blood cell shape	356/39
102	US 57891 19 A	<input checked="" type="checkbox"/>	Image transfer mask for charged particle-beam	430/5

After receiving an event message the full signal is asserted to prevent further queue events as indicated by step 92. The control flow then loops on asserting the event bus request as indicated by step 94 and waiting for a grant as determined in step 96. If a flush is received while waiting for a grant as determined in step 98, the request is deasserted as indicated by step 106 and the full signal is deasserted as indicated by step 108. Flow returns to waiting for a queued message at step 96. When a grant is received as determined at step 100, the queued message is broadcast as indicated by step 100. The request is then deasserted as indicated by step 102. The transmit control then waits for a flush signal as indicated by step 103. Upon receipt of the flush signal, the full signal is deasserted as indicated by step 104 and flow returns to step 90.

A method for controlling the receive queue is illustrated in FIG. 6. The process begins when a cache event message is received from the event bus as indicated by step 110. The control logic asserts its busy signal as indicated by step 112 to prevent further messages from being received until the current operation is complete. After the queued message is executed as indicated by step 114, the conflict signal is sampled as indicated by step 116 and a flush is indicated to the transmit queue if required as indicated by step 120. The final step before returning to step 110 is to deassert the busy signal as indicated by steps 118 and 122.

Having described the preferred embodiments of the invention, other embodiments and variations of the invention will be apparent to those skilled in the art. Therefore, the invention should not be viewed as limited to the disclosed embodiments but rather should be viewed as limited only by the spirit and scope of the appended claims.

What is claimed is:

1. Apparatus for updating a distributed address cache in a switch that transmits a data unit from a first device to a second device in a communications network, comprising:

a first input/output circuit including at least one port operable to receive the data unit, a first cache segment of the distributed address cache operable to store updating said first address cache segment; a second input/output circuit having at least one port, a second cache segment of the distributed address cache operable to store address information, and a first update processor for updating said first address cache segment; and a pathway through which data can be transmitted from said first input/output circuit to said second input/output circuit.

said first update processor circuit being operative to transmit an update message to said second update processor via said pathway prior to updating said first address cache segment, said update message being indicative of changes to be made in the distributed address cache.

2. The apparatus of claim 1 wherein said first address cache segment and said second address cache segment contain substantially identical address information.

3. The apparatus of claim 1 wherein said pathway supports transmission of a single update message at any point in time.

4. The apparatus of claim 3 further including an arbiter for managing control of said pathway by granting control of the pathway to the first input/output circuit in response to a request generated by said first input/output circuit, said arbiter being operative to grant control of said pathway to only one input/output circuit at a time.

5. The apparatus of claim 4 wherein said second input/output circuit asserts a "busy" indicator while processing said update message and said arbiter delays granting control of said pathway in response to assertion of said "busy" indicator.

6. The apparatus of claim 1 wherein said first update processor is operative to facilitate learning a new address from a data unit received via a port of the first input/output circuit by queuing a learn event for transmission via said pathway, and adding an entry for said new address to said first address cache segment once the learn event is transmitted via said pathway.

7. The apparatus of claim 6 wherein said entry includes an ownership indicator that is set to a first state for the address cache segment of the input/output circuit that received the data unit and set to a second state at all other cache segments.

8. The apparatus of claim 7 wherein said entry includes an aging indicator that is set to a first state when said entry is accessed for comparison with a source address.

9. The apparatus of claim 8 further including a scanner that periodically scans the distributed address cache to identify entries where the aging indicator is set to a second state and subsequently rescues the aging indicator in each entry to the second state.

10. The apparatus of claim 9 wherein the first input/output circuit is further operative to queue an event for transmission via said pathway that prompts deletion of said entry through-out the distributed address cache if the entry in the first distributed address cache segment is identified by the scanner to have its aging indicator set to a second state and the ownership indicator in the first distributed address cache segment is set to the first state.

11. The apparatus of claim 1 wherein said first and second I/O circuits contain a receive queue, transmit queue and conflict comparator that detects cache line index matches between said receive and transmit queues.

12. The apparatus of claim 11 wherein said first and second update processors flush update messages stored in the transmit queue when a conflict is detected.

13. A method for updating a distributed address cache in a switch including a first input/output circuit having at least one port and a first cache segment of the distributed address cache, a second input/output circuit having at least one port and a second cache segment of the distributed address cache, and a pathway through which data can be transmitted from said first input/output circuit to said second input/output circuit, comprising the steps of:

receiving a data unit via at least one port of the first input/output circuit;

examining the data unit to determine a source address from the data unit;

searching the first cache segment of the distributed address cache for an entry that is pertinent to the determined source address;

enqueuing an address learn event message for transmission via said pathway if a pertinent entry is not located in said first cache segment; and

adding a new entry to the first cache segment once the address learn event is transmitted via said pathway.

14. The method of claim 13 further including the step of adding a new entry to the second cache segment once the address learn event is transmitted via said pathway.

15. The method of claim 13 further including the step of limiting transmission via said pathway to no more than one message at any point in time.

	Docum ent ID	U	Title	Current OR
103	US 57861 34 A	<input checked="" type="checkbox"/>	Motion picture print film	430/517
104	US 57841 60 A	<input checked="" type="checkbox"/>	Non-contact interferometric sizing of stochastic particles	356/496
105	US 57708 63 A	<input checked="" type="checkbox"/>	Charged particle beam projection apparatus	250/492 .2
106	US 57472 32 A	<input checked="" type="checkbox"/>	Motion imaging film comprising a carbon black-containing backing and a process surviving conductive subbing layer	430/514
107	US 57436 12 A	<input checked="" type="checkbox"/>	Liquid crystal projector	353/97
108	US 57175 18 A	<input checked="" type="checkbox"/>	Broad spectrum ultraviolet catadioptric imaging system	359/357
109	US 57126 85 A	<input checked="" type="checkbox"/>	Device to enhance imaging resolution	348/360
110	US 56795 05 A	<input checked="" type="checkbox"/>	Photographic element useful as a motion picture print film	430/523
111	US 56506 31 A	<input checked="" type="checkbox"/>	Electron beam writing system	250/492 .2
112	US 56400 13 A	<input checked="" type="checkbox"/>	Infrared sensor having a heat sensitive semiconductor portion that detects and absorbs infrared rays	250/338 .4
113	US 56019 67 A	<input checked="" type="checkbox"/>	Blue sensitized tabular emulsions for inverted record order film	430/505
114	US 55944 78 A	<input checked="" type="checkbox"/>	Ink jet recording apparatus for divisionally driving a recording head with a plurality of ink jet orifices grouped into blocks	347/41
115	US 55880 32 A	<input checked="" type="checkbox"/>	Apparatus and method for imaging with wavefields using inverse scattering techniques	378/8
116	US 55878 19 A	<input checked="" type="checkbox"/>	Display device	349/106
117	US 55439 12 A	<input checked="" type="checkbox"/>	Reflectometry of an optical waveguide using a low coherence reflectometer	356/73. 1
118	US 55395 14 A	<input checked="" type="checkbox"/>	Foreign particle inspection apparatus and method with front and back illumination	356/237 .4
119	US 55348 68 A	<input checked="" type="checkbox"/>	Method and system for the detection and measurement of air phenomena and transmitter and receiver for use in the system	342/26
120	US 55176 60 A	<input checked="" type="checkbox"/>	Read-write buffer for gathering write requests and resolving read conflicts based on a generated byte mask code	711/117
121	US 54716 28 A	<input checked="" type="checkbox"/>	Multi-function permutation switch for rotating and manipulating an order of bits of an input data byte in either cyclic or non-cyclic mode	712/223
122	US 54691 76 A	<input checked="" type="checkbox"/>	Focused array radar	342/375
123	US 54628 37 A	<input checked="" type="checkbox"/>	Method of fabricating high density printed circuit board	430/311
124	US 54480 75 A	<input checked="" type="checkbox"/>	Electron-beam exposure system having an improved rate of exposure throughput	250/492 .22
125	US 54384 08 A	<input checked="" type="checkbox"/>	Measuring device and method for the determination of particle size distributions by scattered light measurements	356/336

16. The method of claim 15 further including the step of the first input/output circuit requesting control of said pathway when an event message is generated by the first input/output circuit, said request being processed by an arbiter.

17. The method of claim 16 further including the step of the arbiter granting control of the pathway to the first input/output circuit in response to the request being generated by said first input/output circuit, said arbiter being operative to grant control of said pathway to only one input/output circuit at a time.

18. The method of claim 17 further including the step of said second input/output circuit asserting a "busy" indicator while processing said event message, and the arbiter delaying granting control of said pathway in response to assertion of said "busy" indicator.

19. The method of claim 13 further including the step of designating ownership of said entry by setting an ownership indicator in said entry to a first state for the address cache segment of the input/output circuit that received the data unit.

20. The method of claim 19 further including the step of setting an aging indicator in the entry to a first state when said entry is employed to forward the data unit to the second device.

21. The method of claim 20 further including the step of periodically scanning the distributed address cache to identify entries where the aging indicator is set to a second state and subsequently resetting the aging indicator in each entry to the second state.

22. The method of claim 21 further including the step of the first input/output circuit queuing an event that prompts deletion of said entry throughout the distributed address cache if the entry in the first address cache segment is identified by the scanner and the ownership indicator in the first address cache segment is set to the first state.

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	Document ID	U	Title	Current OR
126	US 54384 05 A	<input checked="" type="checkbox"/>	Device and method for testing optical elements	356/239 .2
127	US 53827 73 A	<input checked="" type="checkbox"/>	Apparatus and method for fabricating a perforated web by light	219/121 .7
128	US 53531 33 A	<input checked="" type="checkbox"/>	A display having a standard or reversed schieren microprojector at each picture element	349/5
129	US 53314 46 A	<input checked="" type="checkbox"/>	Liquid crystal optical element and a laser projection apparatus using polymer dispersed liquid crystal	349/5
130	US 53194 81 A	<input checked="" type="checkbox"/>	Encapsulated liquid crystal optical read/write storage medium and system	349/171
131	US 52989 69 A	<input checked="" type="checkbox"/>	Combined optical train for laser spectroscopy	356/340
132	US 52989 68 A	<input checked="" type="checkbox"/>	Combined optical train for laser spectroscopy	356/338
133	US 52744 20 A	<input checked="" type="checkbox"/>	Beamsplitter type lens elements with pupil-plane stops for lithographic systems	355/67
134	US 52242 14 A	<input checked="" type="checkbox"/>	BuIffet for gathering write requests and resolving read conflicts by matching read and write requests	710/39
135	US 51626 45 A	<input checked="" type="checkbox"/>	Photographic scanner with reduced susceptibility to scattering	250/208 .1
136	US 50981 81 A	<input checked="" type="checkbox"/>	Ophthalmic measuring apparatus	351/221
137	US 50669 97 A	<input checked="" type="checkbox"/>	Semiconductor device	257/211
138	US 50468 47 A	<input checked="" type="checkbox"/>	Method for detecting foreign matter and device for realizing same	356/338
139	US 50400 20 A	<input checked="" type="checkbox"/>	Self-aligned, high resolution resonant dielectric lithography	355/53
140	US 50399 07 A	<input checked="" type="checkbox"/>	Sparkle-free color display	313/478
141	US 50281 35 A	<input checked="" type="checkbox"/>	Combined high spatial resolution and high total intensity selection optical train for laser spectroscopy	356/340
142	US 49881 84 A	<input checked="" type="checkbox"/>	Ophthalmic disease detection apparatus	351/221
143	US 49223 08 A	<input checked="" type="checkbox"/>	Method of and apparatus for detecting foreign substance	356/237 .4
144	US 48988 04 A	<input checked="" type="checkbox"/>	Self-aligned, high resolution resonant dielectric lithography	430/311
145	US 48568 97 A	<input checked="" type="checkbox"/>	Raman spectrometer having Hadamard electrooptical mask and diode detector	356/301
146	US 48283 85 A	<input checked="" type="checkbox"/>	Autolensmeter	356/125
147	US 48213 04 A	<input checked="" type="checkbox"/>	Detection methods and apparatus for non-destructive inspection of materials with radiation	378/86
148	US 47647 76 A	<input checked="" type="checkbox"/>	Thermo transfer printer	347/232

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149	US 46783 25 A	<input checked="" type="checkbox"/>	Apparatus for measuring optical properties of paper	356/73
150	US 46680 89 A	<input checked="" type="checkbox"/>	Exposure apparatus and method of aligning exposure mask with workpiece	356/139 .07
151	US 46424 71 A	<input checked="" type="checkbox"/>	Scattered radiation smoke detector	250/574
152	US 46105 41 A	<input checked="" type="checkbox"/>	Foreign substance inspecting apparatus	356/239 .8
153	US 45989 97 A	<input checked="" type="checkbox"/>	Apparatus and method for detecting defects and dust on a patterned surface	356/237 .5
154	US 44958 17 A	<input checked="" type="checkbox"/>	Ultrasonic imaging device	73/624
155	US 44822 14 A	<input checked="" type="checkbox"/>	Device for applying light to a linear array of magneto-optical light switches, notably for optical printers	359/281
156	US 44213 91 A	<input checked="" type="checkbox"/>	Auto eye-refractometer	351/211
157	US 43558 97 A	<input checked="" type="checkbox"/>	Near-simultaneous measurements at forward and back scatter angles in light scattering photometers	356/338
158	US 43259 10 A	<input checked="" type="checkbox"/>	Automated multiple-purpose chemical-analysis apparatus	422/64
159	US 43242 58 A	<input checked="" type="checkbox"/>	Ultrasonic doppler flowmeters	600/455
160	US 42265 33 A	<input checked="" type="checkbox"/>	Optical particle detector	356/338
161	US 41737 57 A	<input checked="" type="checkbox"/>	Liquid crystal display device	345/50
162	US 41013 83 A	<input checked="" type="checkbox"/>	Process for testing microparticle response to its environment	435/5
163	US 40700 98 A	<input checked="" type="checkbox"/>	Fisheye projection lens system for 35mm motion pictures	359/725
164	US 40506 38 A	<input checked="" type="checkbox"/>	Radioactive matter containing waste gas treating installation	241/222
165	US 39725 98 A	<input checked="" type="checkbox"/>	Multifaceted mirror structure for infrared radiation detector	359/853
166	US 39281 40 A	<input checked="" type="checkbox"/>	Apparatus and process for testing microparticle response to its environment	435/32
167	US 38389 08 A	<input checked="" type="checkbox"/>	GUIDED LIGHT STRUCTURES EMPLOYING LIQUID CRYSTAL	349/19
168	US 37604 71 A	<input checked="" type="checkbox"/>	METHOD OF MAKING AN ELECTROMECHANICAL FILTER	29/25.3 5
169	US 37448 78 A	<input checked="" type="checkbox"/>	LIQUID CRYSTAL MATRIX WITH CONTRAST ENHANCEMENT	349/177
170	US 37137 43 A	<input checked="" type="checkbox"/>	FORWARD SCATTER OPTICAL TURBIDIMETER APPARATUS	356/338
171	US 36472 79 A	<input type="checkbox"/>	COLOR DISPLAY DEVICES	349/23



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